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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,008	07/03/2002	Gilbert Wolrich	10559-311US1 / P9632US	5753

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
06/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/070,008	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-8,10-13,17,19-22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) *2,5,9,14-16,18 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8,10-13,17,19-22 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :02/28/02, 06/09/04, 12/06/04, 12/13/04, 03/07/07, 05/01/07.

1. Claims 1,3, 4,6-8,10,11,12, 13,17, 19-22 ,24-26 are presented for examination. Claims 2,5,9,14-16,18,23 have been canceled.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claim 1, 17, 22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The reasons are given below.

3. As to claims, 1,17,22, although applicant recites a method operating on a processor, the structural elements are not being reflected into the claim body. Therefore, the processor is read as a general arrangement of element. Although applicant further recites executing the branch instruction including a first token specifying the number of instructions that are after the branch and before performing the branch and a second token to cause the processor to prefetch an instruction for the branch taken rather than the sequential instruction if the first token specifies zero or one instruction to execute after the branch , prior to performing an evaluation of a branch condition, it is read as an intended result. The reason is that no actual performance of branch, nor the actual prefetch has been taken place. Therefore, it is non-statutory.

4. As to claim 17,althought claim 17 reciting executing a branch instruction that causes a branch operation in instruction stream deferring performance of branch before performing branch, and evaluating the second token if the first token specifies zero or one instruction, no final result can be found. No actual prefetch has been taken place. Based on broadest interpretation, the "executing a branch instruction that causes..." is an intended use. Therefore, non-statutory.

5. As to claim 22, claim 22 additionally disclosed decode logic. However, logic is an abstract idea. Although the preamble recites "processor", no components of processor have been reflected into the claim body.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,3, 4,6-8,11,12, 13,17, 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (5,517, 628) in view of Peters et al. (4,606,025).

7. As to claims 1,4,12, 13,17, 22, Morrison taught at least executing a branch instruction of an instruction stream with a branch instruction including a first token specifying an amount of delay time, or deferring the performance (see delay field in col.43, lines 6, 17-26, see the amount of time that can be continued after receipt of branch in col.44, lines 61-67, col.45, lines 1-12) that are after the branch instruction to

execute before performing the branch operation and a second token (see condition code field in col.43, lines 17-26, col.44, lines 51-55) that specifies a branch guess operation (branch taken) to prefetch an instruction for the branch taken rather a next sequential instruction if the first token specified zero or one instruction to execute after the branch (see the non-zero and zero value of the delay field in col.45, lines 1-34, see the basic block as the sequential instructions) .

8. Morrison did not specifically show his delay time was a number of instructions as claimed. However, Peters taught a routine for calculating a delay between instructions based the type and the number of instructions (see col.18, lines 47-58). It would have been obvious to one of ordinary skill in the art to use Peters in Morrison for including the number of instructions as clamed because the use of Peters could provide Morrison the ability to convert the delay cycles into number of instructions , and therefore, prefetch the instruction based on the number of instructions, and it could be readily achieved by predefining the instruction number conversion parameters of Peters into the configuration file of Morrison so that specific number the instructions corresponding the delay time could be recognized by Morrison, and because Morrison also taught delivering instructions in a predetermined order (see col.25, lines 9-15), which was a suggestion of the need for determining the number of instructions in order to obtain the instruction block boundaries (see also col.25, lines 23-27), in doing so , provided a motivation.

9. As to claim 3, Morrison also taught optional token (see pipeline stages in col.46, lines 35-67).

10. As to claims 6,7,19-21, Morrison also taught that his invention was also applicable to any number of programmable languages, such as FORTRAN, COBOL, PASCAL, BASIC, etc (see col.21, lines 24-35, see also the compiler 100 in col.14, lines 53-60). Therefore, tokens specified by programmer was applicable.

11. As to claim 8, see col.42, lines 15-26 for unconditional branch.

12. As to claim 11, see context in fig.19 in the instruction register 1900, see also the context CCml in fig.20.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (5,517, 628) in view of Peters et al. (4,606,025) and as applied to claim 1 above, and further in view of Khim Yeoh et al. (5,274,770).

14. As to claim 10, limitation of the parent claim 1 have been discussed in previous paragraph, therefore, it will not be repeated herein. Neither Morrison nor Peters specifically showed the match or mismatch of the byte compare value as claimed. However, Khim Yeoh disclosed a system for performing a conditional branch based a comparison of values in bytes (see col.3, lines 15-18). It would have been obvious to one of ordinary skill in the art to use Khim Yeoh in Morrison for including the match and mismatch (i.e. comparison) of the byte compare value as claimed because the use of Khim Yeoh could expand the processing structure of Morrison to accept additional conditional parameters, such as the conditional code of certain width, thereby enhancing the compatibility of the system bus, and because Morrison also taught petitionable instruction cache (see col.34, lines 4-18), which was an indicating of the applicability of byte or word value.

15. Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (5,517, 628) in view of Peters et al. (4,606,025) and as applied to claims 1, 17, 22 above, and further in view of Chrysos (5,923,872).

16. As to claims 24-26, neither Morrison nor Peters specifically teach the hardware based multi threaded as claimed. However, Chrysos disclosed a system including hardware contexts for simultaneously multithreaded execution (see co1.12, lines 15-18). It would have been obvious to one of ordinary skill in the art to use Chrysos in Morrison for including the hardware based multi threaded as claimed because the use of Chrysos could provide Morrison the capability to adjust to specific hardware construct of the branch prediction, and it could be readily achieved by configuring the hardware

parameters of Chrysos (or the contexts) into Morrison so that the specific hardware based multithreads of Chysos could recognized by Morrison, and because Morrison was also directed to the pipelined branch instructions which included hardware functions (see co1.45, lines 53-67, col.46, lines 1-51). As to the hardware base, see the bit level of the condition codes in fig.20.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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